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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,138	07/31/2003	Nick A. Youker	279.659US1	1822

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/632,138	YOUKER ET AL.	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/19/09 has been entered.

Note:

a second end of each capacitor is connected via the interconnect to a constant voltage level (see abstract).

a constant voltage levels such as ground planes (see para 0027).

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification is silent regarding "**each conductive layer**

is electrically connected to a constant voltage to form a constant voltage plane (a grounding plane) (claims 1, lines 8-9), **the multi-laver circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors to provide electrical shielding and wherein one I/O conductor provides an electrical connection to the constant voltage plane**, claim 1, lines 9-12). Nowhere in the specification discloses or describes the limitation as claimed as above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 8-12, 15-18, and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hitman et al. (267) in view of Truex et al. (U.S. Patent 5,683,435).

As to claims 1-5, 15-16, Hittman discloses an apparatus as shown in figures 1-12 comprising:

one or more Input/output (I/0) conductors (12a, 12b), wherein the I/O conductors pass through a hermetic seal (20) such that a first end of the I/O conductors resides on a non-hermetic side of the hermetic seal and a second end of the I/O conductors resides on a hermetic side of the hermetic seal within a hermetically sealed interior of a hermetically sealed metal case of the apparatus;

a printed circuit interconnect substrate (132) residing on the hermetic side of the hermetic seal (20) and is arranged substantially parallel to the seal and normal (perpendicular) to the I/O conductors (see figures 5-7), the substrate is mounted on a hermetic side of the seal (20) and made by ceramic or FR4 material; and

one or more ceramic chip capacitors (110), which are discrete capacitor or surface mount package (claims 15-16) mounted on the printed circuit interconnect substrate and mounted within the hermetically sealed *the interior of the* metal case *(the capacitors are covered by a seal part 20)*, wherein a first end of each capacitor is electrically connected via printed circuit (trace or wiring or patterns 142, 146) interconnect to the second end of the I/O conductor and a second end of each capacitor is electrically connected via the printed circuit interconnect to the metal case (20, 24, and 26).

Hitman does not specific discloses the printed circuit interconnect substrate includes a multi-layer circuit board comprising a buried signal layer between first and second conductive layers, wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane (a grounding plane).

Truex et al teaches a feed through assembly (10) as shown in figures 1-4 comprising a multilayer circuit board (34) specifically in figure 3 having a signal layer (56) between first and second conductive layers (64, 66), wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane (ground), see column 4, line 59 through column 5, line 62). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of

Truex et al. employed in the apparatus of Hitman in order to reduce noise for the multilayer circuit board.

As to claim 6, Hittman as modified discloses the printed circuit interconnect substrate (132) includes a flexible circuit tape (see figures 6-8).

As to claim 8, Hittman as modified discloses the printed circuit interconnect substrate is a multi-layer substrate (insulating layer and a ground layer).

As to claims 9-12, Hittman as modified discloses the printed circuit interconnect substrate includes an electrically conductive medium, which is a solder or conductive adhesive.

As to claims 17-18, Hittman as modified discloses the capacitors are included in a multi-chip package, and are adapted to filter electromagnetic interference (EMI).

As to claims 23-26, Hittman as modified discloses the I/O conductors that are pins, wires, or conductive traces formed on/in the circuit board.

4. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hittman) and Truex et al, and further in view of Brendel et al. (U.S. Patent 6,529,103).

Regarding claims 19-22, Hittman and Truex et al. do not disclose the hermetic seal is a part of an implantable medical device and the seal material including a ceramic, epoxy, or glass.

Brendel et al teaches an improved internally ground feed through capacitor comprising a hermetic seal is a part of an implantable medical device and the seal material including a ceramic, epoxy, or glass, see column 1, lines 30-62.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Brendel et al. employed in the apparatus of Hittman and Truex in order to reduce cost and prevent the ingress of body fluids of implanted devices, and also, the hermetic seal material made by ceramic, epoxy, or glass is suitable for withstanding high temperature and thermal stress.

5. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hittman and Truex, and further in view of Andresakis et al. (U.S. Patent 6,657,849).

As to claims 13-14, Hittman and Truex do not disclose the capacitors having a dielectric breakdown voltage of about 1200 volts, or within a range of about 200 to 1500 volts.

Andresakis et al. shows a capacitor having a dielectric breakdown voltage of about 1200 volts, or within a range of about 200 to 1500 volts, see examples 1-5.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Andresakis et al. employed in the apparatus of Hittman and Truex in order to provide a high quality ceramic EMI/RFI filter capacitor applied in vary of an electronic device.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hittman and Truex, and further in view of Chee (U.S. Patent 6,657,133).

As to claim 7, Hittman and Truex do not disclose the flexible circuit tape includes polyimide tape.

Chee teaches a circuit board made by polyimide tape, column 2, lines 30-61.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Chee employed in the apparatus of Hittman and Truex in order to provide a flexible and high thermal stress for the circuit board.

Response to Arguments

Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues:

a) Truex with Hittman does not teach or suggest "wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors," as recited in claim 1.

Examiner disagrees because as in portion #4 of the Office action, the combination of Hittman as modified by Truex meets the claim limitations.

b) Hittman and Truex fail to disclose "wherein one I/O conductor provides an electrical connection to the constant voltage plane." Examiner disagrees, see portion # 3 for 112, first paragraph rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reichard Dean can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T Dinh/
Primary Examiner, Art Unit 2841.